

Teaching plan
Subject: Computer Science
Paper Code: COM0700404:

Credit/Total no. of classes.3+1
Period: Theory: 45 Hours
Practical: 30 Hours
Non Contact: 5hour

Paper Name: ADVANCED COMPUTER ORGANIZATION AND ARCHITECTURE

Theory
Faculty : P.P.D.Sarma

Lecture No.	Topic	Mode of Teaching (Experiential Learning, Participative Learning)	Teaching Aids use	Assessment Method
1,10	Computer Arithmetic : Serial adder, Parallel adder, Ripple carry adder, Carry look-ahead adder, Multiplication of signed and unsigned numbers, Booth's algorithm, Division of integer, Floating point arithmetic.	Participative Learning	Computer system with overhead projector	QUIZ
11-25	UNIT 2: Advanced Architectures Classification: SISD, SIMD, MISD, MIMD, Bus data path:one, two and three bus, Scalar, vector, superscalar and pipelined processor,VLIW architecture, EPIC architecture, Pipelining: Instruction pipeline, pipeline bubbles, Hazards: resource conflicts, data dependency, branch difficulty, Vector computing: arithmetic pipeline, vector and scalar register, chaining, scatter gather operations, vector-register processor, Memory vector processor, Array processor	Participative Learning	Computer system with overhead projector	QUIZ
25-35	UNIT 3: Assembly Language Machine Language, Register transfer language, Assembly Language, Assembler, Program Loops, Subroutines, Developing counters and Time delay routines, Input-Output Programming. Interfacing concepts.	Participative Learning	Computer system with overhead projector	QUIZ
36-41	UNIT 4: 8085 Microprocessor Architecture and Memory Interface 10 Pin Description, Operating Modes, Instruction Set of 8085: Instructionset, Data	Participative Learning	Computer system with overhead projector	QUIZ

	formats, Addressing modes, Opcode & Operands, Data and Storage, Word size, 8085 Instructions: Counter and Time delays, Stack, Subroutines, Call & Return statements, Interrupts in 8085: generation of RST codes, interrupt priority, SIM & RIM instructions.			
42-47	UNIT 5: Multiprocessor Characteristics of Multiprocessors, Interconnection Structures, Interprocessor Arbitration, Interprocessor Communication and Synchronization, Cache Coherence, Multicore Processors	Participative Learning	Computer system with overhead projector	QUIZ
48-55	UNIT 6: Dataflow Computers and VLSI Computations Data flow architecture: static and dynamic, VLSI Computing Structures, Array Architectures, Mapping algorithms, Reconfigurable processor array, VLSI matrix arithmetic models and processors, Matrix Algorithms and Pipelines	Participative Learning	Computer system with overhead projector	QUIZ

8085 Training kit will be used